REMARKS

In an Office Action mailed on February 22, 2006, the Examiner: (1) noted that a certified copy of a priority application has not been filed; (2) reiterated a request to provide the "Summary of the Invention" section; (3) rejected claims 1-3, 14-18, and 23 under 35 U.S.C. § 102(b) as being anticipated by Gupta (U.S. Pat. No. 6,163,877); and (4) rejected claims 4-13, 19-24, and 28-29 under 35 U.S.C. § 103(a) as being obvious based on a combination of Gupta and Aoki (U.S. Pat. No. 5,675,501).

Concerning the certified copy of the priority application, PCT/RU02/00430, Applicants filed the certified copy on February 23, 2006. Accordingly, Applicants respectfully request the Examiner to acknowledge the receipt of the certified copy.

Regarding the request to provide the "Summary of the Invention," although Applicants respectfully disagree with the Examiner's requirement, for at least the reasons given in the Amendment filed on December 7, 2005, to expedite prosecution, by this Amendment, Applicants amend the Specification to provide a Summary of the Invention section. No new matter has been added, since the paragraph included as the Summary of the Invention includes the contents of the Abstract of the Disclosure section. Accordingly, Applicants respectfully request the Examiner to enter this Amendment to the Specification and withdraw the objection to the Specification.

With respect to the rejection of claims 1-3, 14-18, and 23 under 35 U.S.C. § 102(b) as being anticipated by Gupta, Applicants respectfully traverse the rejection for at least the reasons given below. Taking claim 1 as being exemplary, claim 1 is related to a method for generating an integrated circuit layout, including folding only one of the widest transistors to produce a folded transistor that is electrically equivalent to the widest transistor, the folded transistor having at least two fingers, each finger having a smaller width than the width of the widest transistors and creating a fold solution for the layout with the one folded transistor. In contrast, Gupta teaches folding all transistors. The folding process taught by Gupta, as discussed with respect to Figure 9 clearly teaches folding all large transistors. (See item 906 of Figure 9). Specifically, Gupta describes the folding step, step 906, as:

> Referring again to FIG. 9, at step 906 large transistors are folded. Large transistors are defined by the user as transistors exceeding a certain height. Large transistors thus defined are folded at this stage as many times as necessary in order for individual folds to be under a maximum height specified by the user. According to this

> embodiment, transistors can be folded at this stage into either an even number of folds or an odd number of folds.
>
> Gupta, col. 7, ll. 33-40.

Thus, Gupta teaches folding all large transistors, which are defined as those transistors whose height exceeds a user defined criteria.

As to the parts of Gupta relied upon by the Examiner to reject claim 1, Gupta shows in Figure7A three transistors N1, N2, N3, each of which is folded, as shown in Figure 7B. (See Figures 7A-B and col. 5, ll. 40-65). The corresponding discussion in the Gupta specification confirms this; as it states "[f]or layout 702, each transistor N1, N2, and N3 is folded into three folds." col. 5, ll. 64-65. Gupta is primarily concerned with avoiding a disadvantage of the prior art related to folding a transistor into even number of folds. (col. 5, ll. 39-42). Folding of transistors created lack of sharing of diffusion layer among transistors, which could be addressed by interlacing. Apparently, prior to Gupta, interlacing was done manually after the integrated circuit layout process was complete. To address this problem, Gupta teaches a process that incorporates interlacing automatically in a layout process. (col. 5, ll. 44-47). Concerning Figure 5 of Gupta, which shows a transistor F as being folded, Applicants respectfully note that Figure 5 and related discussion merely discuss the effect of folding on diffusion sharing. (col. 3, ll. 31-32; col. 4, ll. 44-67). In particular, Gupta notes that despite transistor F being folded it cannot share a diffusion layer with transistor E. (See 504 in Figure 5). The process taught by Gupta, however, requires that all large transistors be folded, as discussed above. Thus, Gupta nowhere teaches folding only one of the widest transistors to produce a folded transistor and creating a fold solution with the one folded transistor. Accordingly, at least for this reason Applicants respectfully request the Examiner to withdraw the rejection of claim 1.

Claims 2 and 3 depend, directly or indirectly, from claim 1 and thus are patentable for at least the reasons given above with respect to claim 1.

Claim 14 is also patentable because for at least similar reasons as given above with respect to claim 1, Gupta does not teach a method for generating an integrated circuit layout including iteratively folding only one transistor at a time of the plurality of transistors that have a width greater than a predetermined width to produce two transistors, each of the two transistors having a width shorter than the width of a corresponding unfolded transistor and after each iteration, creating a fold solution after each iteration and adding the fold solution to a fold solution list.

Claims 15-18 depend, directly or indirectly, from claim 14 and thus are patentable for at least the reasons given above with respect to claim 14.

Concerning the rejection of claims 4-8 under 35 U.S.C. § 103(a) as being obvious based on a combination of Gupta and Aoki, Applicants respectfully submit that the Examiner has failed to establish a prima facie case of obviousness. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. M.P.E.P. § 2143. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Each of claims 4-8 depends, directly or indirectly, from claim 1 and thus is patentable for at least the reasons given above with respect to claim 1. Moreover, Aoki does not cure the deficiencies of teachings of Gupta. In particular, Aoki does not teach or suggest folding only one of the widest transistors to produce a folded transistor that is electrically equivalent to the widest transistor, the folded transistor having at least two fingers, each finger having a smaller width than the width of the widest transistors and creating a fold solution for the layout with the one folded transistor. Thus, even if combined with Gupta (which it cannot be), Aoki does not teach or suggest the subject matter of claims 4-8. Accordingly, Applicants for at least these reasons seek allowance of claims 4-8, as well.

Regarding the rejection of claims 19-22 under 35 U.S.C. § 103(a) as being obvious based on a combination of Gupta and Aoki, Applicants respectfully submit that the Examiner has failed to establish a prima facie case of obviousness. Each of these claims depends, directly or indirectly, from claim 14 and thus is patentable for at least the reasons given above with respect to claim 14. Moreover, Aoki does not cure the deficiencies of teachings of Gupta. In particular, Aoki does not teach or suggest iteratively folding only one transistor at a time of the plurality of transistors that have a width greater than a predetermined width to produce two transistors, each of the two transistors having a width shorter than the width of a corresponding unfolded transistor and after each iteration, creating a fold solution after each iteration and adding the fold solution to a fold solution list. Thus, even if combined with Gupta (which it cannot be), Aoki

does not teach or suggest the subject matter of claims 19-22. Accordingly, Applicants for at least these reasons seek allowance of claims 19-22, as well.

With respect to the rejection of claims 9-13, 23, 28, and 29 under 35 U.S.C. § 103(a) as being obvious based on a combination of Gupta and Aoki, Applicants respectfully submit that the Examiner has failed to establish a prima facie case of obviousness. In particular, regarding claim 9, Applicants respectfully submit that Gupta does not teach folding transistors of the dependent pairs having a height lower bound greater than a predetermined amount to produce an N-channel dependent fold list and a P-channel dependent fold list and merging the list of folded N-channel transistors, the list of folded P-channel transistors, the N-channel dependent fold list and the P-channel dependent fold list to produce an initial fold solution list. In contrast, Gupta teaches folding large transistors in step 906, prior to forming pairs. The Examiner relies on step 908 of Figure 9 to conclude that Gupta teaches folding transistors of the dependent pairs having a height lower bound greater than a predetermined amount to produce an N-channel dependent fold list and a P-channel dependent fold list and merging the list of folded N-channel transistors, the list of folded P-channel transistors, the N-channel dependent fold list and the P-channel dependent fold list to produce an initial fold solution list. Applicants respectfully disagree with the Examiner's characterization of the teachings of Gupta at least because Gupta merely teaches forming pairs of transistors, once they have already been folded. As part of step 908, Gupta teaches pairing P/N pairs using a set of prioritized criteria, including "gate signals, least difference in the number of folds, membership in the same cluster, and common diffusion terminals." (col. 7, ll. 44-50). That step, however, occurs after all of the large transistors have been folded individually without reference to any pairing in step 906 (See Figure 9). Thus, Gupta does not teach or suggest teach folding transistors of the dependent pairs having a height lower bound greater than a predetermined amount to produce an N-channel dependent fold list and a P-channel dependent fold list and merging the list of folded N-channel transistors, the list of folded P-channel transistors, the N-channel dependent fold list and the P-channel dependent fold list to produce an initial fold solution list.

Aoki does not cure the deficiencies of teachings of Gupta, and thus even if it is combined with Gupta, Aoki does not teach or suggest the subject matter of claim 9. Aoki is directed to a method for designing a transistor module 60 including transistor rows 61, 62, and 63, as shown in Figure 2. (col. 5, ll. 1-21). As part this method, Aoki teaches a seven step process, as shown

in Figure 3. The process includes: (1) placing transistors corresponding to the transistor module 60; (2) calculation of size of each of the transistor rows in X direction and Y direction; (3) determination of the size of the transistor module in the X direction; (4) determination of the size of the transistor rows in the Y direction, including folding transistors, if necessary; and (5) arranging the transistors rows in parallel. (See Figure 3). As part of the step relating to the determination of the size of the transistor rows in the Y direction, Aoki describes a method for calculating a modified size, Tw2, in the Y direction for the transistors. No where, however, Aoki teaches or suggests folding transistors of the dependent pairs having a height lower bound greater than a predetermined amount to produce an N-channel dependent fold list and a P-channel dependent fold list and merging the list of folded N-channel transistors, the list of folded P-channel transistors, the N-channel dependent fold list and the P-channel dependent fold list to produce an initial fold solution list. Accordingly, at least for these reasons, Applicants respectfully request the Examiner to withdraw the rejection of claim 9.

Claims 10-13 depend, directly or indirectly, on claim 9 and thus are patentable for at least the reasons given above with respect to claim 9.

Concerning claim 19, Applicants respectfully submit that the combination of Gupta and Aoki fails to teach or suggest folding transistors of the dependent pairs having a height lower bound greater than a predetermined amount to produce an N-channel dependent fold list and a P-channel dependent fold list and merging the independent N-channel fold solution list, the independent P-channel fold solution list, the N-channel dependent fold list and the P-channel dependent fold list to produce an initial fold solution list for at least the reasons given above with respect to claim 9. Claims 20-22 depend, directly or indirectly, on claim 19 and thus are patentable for at least the reasons given above with respect to claim 19.

Regarding claim 23, Applicants respectfully submit that the combination of Gupta and Aoki fails to teach or suggest folding the widest transistors of the plurality of N-channel transistors and the plurality of P-channel transistors to produce a list of folded N-channel transistors and a list of folded P-channel transistors, wherein the list of folded N-channel transistors and the list of folded P-channel transistors are produced independent of the dependency map and merging the list of folded N-channel transistors, the list of folded P-channel transistors, the N-channel dependent fold list and the P-channel dependent fold list to produce an initial fold solution list for at least the reasons given above with respect to claim 9. Claims 28

and 29 depend, directly or indirectly, on claim 23 and thus are patentable for at least the reasons given above with respect to claim 23.

The Office Action contains numerous statements characterizing the claims, the specification, and the prior art. Regardless of whether such statements are addressed by Applicants, Applicants refuse to subscribe to any of these statements, unless expressly indicated by Applicant. Should issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 996-6839. If Applicants have overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

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